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(54) MAGNETIC REPRODUCING AND DECODING DEVICE

(57)Abstract:

PURPOSE: To obtain an accurate stable clock, and to enable complete follow-up to the change of a data rate by controlling the sampling lock of an A/D converter by a phase error output.

CONSTITUTION: A reproducing signal integrated and equalized by an integrating equalizer 115 is quantitized by converting the signal level of the reproducing signal while using a synchronous clock of twice as large as a data rate as a reference by an A/D converter 116. A phase error detector 1 is supplied with the quantitized reproducing signal. A signal inverted by the polarity of before odd data is D/A converted and extracted as a phase error signal at the time of the reverse polarity of before and after odd data in the even sample data of quantitized digital data. That is, a gate is worked and no error signal is output at the time of the same polarity of the before and after odd data. A high-accurary synchronous clock is obtained by a voltage-controlled oscillator 9 regarding the phase error signal. Accordingly, the reproducing signal is quantitized by the clock completely synchronized with the signal after integrating and equalization, and partial response conversion and Viterbi decoding are conducted, thus perfectly following up the change of

the data rate.

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CLAIMS

[Claim(s)]

[Claim 1] The integral equalizer which carries out integral equivalence of the RF signal reproduced by the playback means, The A/D converter which quantizes the output of the above-mentioned integral equalizer with a twice as many clock as a data rate, The partial response converter changed into the partial response which shows the predetermined band pass frequency characteristics by the intersymbol interference to odd number sample data among the outputs of the above-mentioned A/D converter, The decoder which

decodes playback data from the output of the above-mentioned partial response transducer, Only when the polarity of the odd number sample data of order is reversed from the output of the above-mentioned A/D converter to even number sample data, it multiplies with the polarity of front odd number sample data. It has the phase error detector which calculates a phase error, and the voltage-controlled oscillator which controls the clock of the above-mentioned A/D converter based on the phase error of the above-mentioned phase error detector. Magnetic-reproducing decode equipment characterized by controlling the sampling clock of the above-mentioned A/D converter by this phase error output.

[Claim 2] Magnetic-reproducing decode equipment characterized by forming the above-mentioned A/D converter and the 2nd A/D converter which operates with the sampling clock of opposition in magnetic-reproducing decode equipment according to claim 1, quantizing to odd number sample data with the above-mentioned A/D converter, and quantizing to even number sample data with the 2nd A/D converter of the above.

[Claim 3] The above-mentioned partial response transducer is magnetic-reproducing decode equipment characterized by making it change into other partial responses which show other predetermined band pass frequency characteristics according [on magnetic-reproducing decode equipment according to claim 1 and / as opposed to / among the outputs of the above-mentioned A/D converter / odd number sample data] to an intersymbol interference.

[Claim 4] In magnetic-reproducing decode equipment according to claim 1 the above-mentioned phase error detector The inverter circuit which reverses the above-mentioned even number sample data from the output of the above-mentioned A/D converter to even number sample data only when the polarity of the odd number sample data in front of 1 sample is plus, The D/A converter which changes into an analog signal the above-mentioned even number sample data reversed in the above-mentioned inverter circuit, It has the gate circuit which carries out the gate of the analog signal from the above-mentioned D/A converter only when the polarity of the odd number sample data before and behind the above-mentioned even number sample is

reversed. Magnetic-reproducing decode equipment characterized by detecting a phase error and changing the sequence of the above-mentioned inverter circuit, the above-mentioned D/A converter, and the above-mentioned gate circuit into arbitration from the above-mentioned gate circuit.

[Claim 5] Magnetic-reproducing decode equipment characterized by preparing the quantization feedback circuit which carries out low-pass amendment of a regenerative signal from the output of the above-mentioned integral equalizer in magnetic-reproducing decode equipment according to claim 1.

[Claim 6] Magnetic-reproducing decode equipment characterized by having changed to the above-mentioned integral equalizer and forming the digital equalizer which carries out equivalence of the output of the above-mentioned A/D converter to the 1st criteria of nyquist in magnetic-reproducing decode equipment according to claim 1.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention is used for a digital video tape recorder, and relates to suitable magnetic-reproducing decode equipment.

[0002]

[Description of the Prior Art] Conventionally, in VTR, coding of a record signal, i.e., channel coding, was performed. Channel coding means changing a sign into the gestalt suitable for the property of a record reversion system. In order to specifically record the digital sign which has a low-frequency component on the magnetic-recording reversion system which cannot reproduce a direct current or a low-frequency component, he is trying to oppress the low-frequency component of a digital sign.

[0003] Many approaches of channel coding of VTR are proposed. In this, an NRZI code and especially an INTARIBUDO NRZI code are called partial

response sign. In recent years, the partial response (PR) developed in the communication link field and to apply the partial response class 4 (PR4) especially are tried.

[0004] As a PR equivalence method, PR (1 -1) and PR (1, 0, -1) are known. PR (1 -1) correspond to an NRZI code, and PR (1, 0, -1) correspond to an INTARIBUDO NRZI code. PR (1 -1) and PR (1, 0, -1) -- it both becomes 3 value wave at a detecting point at the time of playback. Here, the integer shown in a parenthesis expresses the multiplier of the filter as a digital filter which constitutes PR equalizer.

[0005] As an equivalence method, when PR (1 -1), i.e., an NRZI code, are used, there are few direct currents and low-frequency components, and the frequency characteristics of a high pass mold are shown. The frequency characteristics of PR (1 -1) are (1-D) (however, D shows the delay operator of bit period T.), and the intersymbol interference which has the value of -1 following an isolated pulse produces them.

[0006] On the other hand, as an equivalence method, when PR (1, 0, -1), i.e., an INTARIBUDO NRZI code, are used, there are both few RFs and low-frequency components, and the cycle property of a band pass mold is shown. The frequency characteristics of PR (1, 0, -1) are (1-D2), and the intersymbol interference which has the value of -1 2 bits after an isolated pulse produces them.

[0007] Thus, application of a partial response has the intention of operating a playback frequency orthopedically at a detecting point, using an intersymbol interference positively. Since it is close to a magnetic-recording property, especially an INTARIBUDO NRZI code (1, 0, -1), i.e., PR, application to an old digital video tape recorder is tried, and it is made to have the video signal reproduced efficiently.

[0008] The frequency characteristics (1-D2) of PR (1, 0, -1) can be decomposed into - (1-D) (1+D). Generally, a property (1-D) is executed by proxy in the differential property at the time of playback, and a property (1+D) is realized by performing 1-bit analog delay and addition processing. (1+D) The original sign can be decoded, if "1" after conversion of a three values wave and "-1" are identified to "1" and "0" is identified to "0." A timing signal

can be extracted from a wave including the RF signal after conversion (1-D).

[0009] Generally, in order to avoid propagation of the digital error at the time of decode, the signal-processing system which applied the partial response sign has PURIKODO which changes input data into a middle sequence, a magnetic-recording system, and a multiple-value discrimination decision circuit, and multiple-value discernment of the input data is carried out, and it is decoded. Below, an example is described.

[0010] Drawing 16 is the block diagram of the digital video signal processor for which the applicant of this invention applied previously. This digital video signal processor has the recording system 100 which records data on a magnetic tape 106, and the reversion system 107 which reproduces the data recorded on the magnetic tape 106.

[0011] A recording system 100 has A/D converter 101, SHAFURU and the band compression circuit 102, the parity addition circuit 103, the 1 / (1-D2) PURIKODO circuit 104, and a recording head 105 in order to record a video signal on a magnetic tape 106.

[0012] A reversion system 107 is circuitry contrary to a recording system 100, and it has the reproducing head 108, the decoding (1-D2) circuit 109, the error detection correction circuit 110, band expanding and DESHAFURU 111, and D/A converter 112 in order to reproduce the video signal recorded on the magnetic tape 106.

[0013] If what has a property (1-D2) is used as a decoding circuit 109 in a reversion system 107 as a PURIKODO circuit 104 in a recording system 100 using what has a 1-/(1-D2) property, this digital video signal processor will turn into a digital video signal processor which applied the partial response class 4 (PR4).

[0014] Thus, the constituted digital video signal processor carries out the following actuation. In a recording system 100, A/D converter 101 supplies and quantizes and an input video signal is changed into a digital video signal. This digital video signal is supplied to SHAFURU and the band compression circuit 102, and carries out and carries out shuffling of a discrete cosine transform and the Huffman coding processing per predetermined block about a digital video signal. The digital video signal by which shuffling was carried

out is supplied to the parity addition circuit 103, and the parity for error corrections is added. PURIKODO [it / the digital video signal with which the parity for error corrections was added is supplied to the 1-/(1-D2) PURIKODO circuit 104, and / the partial response class 4 (PR4)]. The digital video signal [PURIKODO / video signal] is recorded on a magnetic tape 106 through a recording head 105.

[0015] In a reversion system 107, the video signal recorded on the magnetic tape 106 is reproduced by the reproducing head 108, and the reproduced high frequency signal is supplied to the decoding (1-D2) circuit 109, and is decoded. the decoded data are supplied to the error detection correction circuit 110 -- having -- error detection -- and an error correction is carried out. Error detection and the data by which the error correction was carried out are supplied to band expanding and DESHAFURU 111, and band expanding and DESHAFURU are performed. The data [DESHAFURU / data / which were DESHAFURU and were band-elongated] are supplied to D/A converter 112, and are changed into an output video signal.

[0016] Drawing 17 is drawing showing PR4 playback decoder circuit for which the applicant of this invention applied previously. The RF signal reproduced by the reproducing head 108 is supplied and amplified by amplifier 113. The reproducing head 108 and amplifier 113 are formed on the rotating drum which is not illustrated. The regenerative signal amplified with amplifier 113 is supplied to the rotary transformer 114, and is taken out besides a rotating drum. The regenerative signal taken out besides the rotating drum through the rotary transformer 114 is supplied to the integral equalizer 115, and performs data processing of integral identification, i.e., (1+D). Thereby, identification of the regenerative signal is carried out to the 1st criteria of nyquist. One side of the regenerative signal by which integral identification was carried out is supplied to A/D converter 116, on the basis of a synchronous clock, changes the signal level of a regenerative signal into digital value, and quantizes.

[0017] The quantized digital data is supplied to a computing element (1-D2) 117, and identification is carried out to the partial response class 4 (PR4). Viterbi decoding of the data by which identification was carried out to the partial response class 4 (PR4) is supplied and carried out to the Viterbi

decoder 118. Viterbi decoding is a decode method which obtains playback data from the pattern of all state transitions in search of the pattern of a state transition with the highest possibility to a regenerative signal.

[0018] In VTR using Viterbi decoding, a bit error rate can be improved by decoding a regenerative signal, using the intersymbol interference of input data effectively in the Viterbi decoder.

[0019] Here, another side of the regenerative signal by which integral identification was carried out is supplied to a limiter 119. The zero cross later mentioned by this limiter 119 is detected, and the clock component to a zero cross is extracted. This clock component is supplied to the PLL circuit 120, and the synchronous clock which synchronized with the integral identification output is generated. It is made to sample the data in A/D converter 116, a computing element (1-D2) 117, and the Viterbi decoder 118 with this synchronous clock, applying phase simulation. This becomes possible also to fluctuation of not only the jitter of VTR but the data rate at the time of a search to obtain an exact and stable clock.

[0020] Drawing 18 is drawing showing the signal wave form of PR4 playback decoder circuit for which the applicant of this invention applied previously. PURIKODO output as 1 / (1-D2) PURIKODO circuit 104 shown in drawing 16 are PURIKODO the record data shown in drawing 18 A and shown in drawing 18 B It obtains. Moreover, 2-bit delay of a PURIKODO output comes to be shown in drawing 18 C. The output from the reproducing head 108 shown in drawing 17 comes to be shown in drawing 18 D. The output of the integral equalizer 115 shown in drawing 17 comes to be shown in drawing 18 E. And a playback clock as shown in drawing 18 F from this equalizer output is extracted. Moreover, 2-bit delay of an integral equalizer output comes to be shown in drawing 18 G. The output of the computing element 117 shown in drawing 17 (1-D2) serves as 3 value wave, as shown in drawing 18 H.

[0021] Drawing 19 is drawing showing the eye pattern of PR4 playback decoder circuit for which the applicant of this invention applied previously. An eye pattern says drawing which wrote the regenerative-signal wave after identification in piles the detecting point period (data rate), and the situation of the intersymbol interference of an identification signal is investigated. The eye

pattern which the eye pattern shown in drawing 19 A shows the eye pattern after the integral identification by the integral equalizer 115 shown in drawing 17 , and is shown in drawing 19 B shows the eye pattern after the identification by the computing element 117 shown in drawing 17 (1-D2) (1-D2). The limiter 119 shown in drawing 17 is generating the synchronous clock by detecting this zero cross.

[0022] Drawing 20 is drawing showing the actual configuration of PR4 playback decoder circuit for which the applicant of this invention applied previously. In drawing 20 , after the regenerative signal by which integral identification was carried out with the integral equalizer 115 is supplied to the delay circuit 121 and carries out specified quantity delay of the regenerative signal of a main track system, it is made to be supplied to A/D converter 116. Other configurations are the same as that of what was shown in drawing 17 .

[0023] Drawing 21 is drawing showing the amount of delay in the actual configuration of PR4 playback decoder circuit for which the applicant of this invention applied previously. An integral equalizer output is shown in drawing 21 A, a limiter output is shown in drawing 21 B, a PLL circuit output is shown in drawing 21 C, and an A/D-converter output is shown in drawing 21 D. In such an actual circuit, as for the limiter output shown in drawing 21 B, only d1 is delayed from the zero crossing point of the integral equalizer output shown in drawing 21 A as transfer time. Moreover, only d2 is further delayed for the limiter output which shows the PLL circuit output shown in drawing 21 C to drawing 21 B as transfer time. Furthermore, only d3 is delayed as strobe delay in an A/D converter to the PLL circuit output which shows the A/D-converter output shown in drawing 21 D to drawing 21 C. Thus, in a clock extract path, a synchronous clock is delayed from the integral equalizer 115 by only d4 even to A/D converter 116. Therefore, the sampling point in A/D converter 116 will shift. He generates this amount d4 of delay in the delay circuit 121, and is trying to delay the regenerative signal of a main track system.

[0024]

[Problem(s) to be Solved by the Invention] Thus, the limiter [in / in the conventional PR4 playback decoder circuit / a clock extraction system] 119

and the amount of delay by the transfer time of the PLL circuit 120, It is necessary to the amount of delay by the strobe delay in an A/D converter to form the delay circuit 121 which amends this in a main track system. Adjustment for that was needed and there was un-arranging [that the stability on the temperature characteristic over each amounts d1, d2, and d3 of delay mentioned above also posed a problem further].

[0025] This invention is made in view of this point, and does not receive effect in a time delay, stability, etc. of a clock extraction system, but aims at offer of the magnetic-reproducing decode equipment which obtains an exact clock.

[0026]

[Means for Solving the Problem] The integral equalizer 115 which carries out integral equivalence of the RF signal reproduced by the playback means 108 as the magnetic-reproducing decode equipment of this invention is shown in drawing 1 thru/or drawing 15 , A/D converter 116 which quantizes the output of the integral equalizer 115 with a twice as many clock as a data rate, The partial response converter 117 changed into partial response class 4PR (1, 0, -1) from the 1st criteria of nyquist to odd number sample data among the outputs of A/D converter 116, The decoder 118 which decodes playback data from the output of the partial response transducer 117, Only when the polarity of the odd number sample data of order is reversed from the output of A/D converter 116 to even number sample data, it multiplies with the polarity of front odd number sample data. It has the phase error detector 1 which calculates a phase error, and the voltage-controlled oscillator 9 which controls the clock of A/D converter 116 based on the phase error of the phase error detector 1, and the sampling clock of A/D converter 116 is controlled by this phase error output.

[0027] Moreover, as shown in drawing 1 thru/or drawing 15 , the magnetic-reproducing decode equipment of this invention forms A/D converter 116 and 2nd A/D converter 11 which operates with the sampling clock of opposition, quantizes to odd number sample data with A/D converter 116, and is made to quantize with 2nd A/D converter 11 in **** to even number sample data.

[0028] Moreover, the magnetic-reproducing decode equipment of this invention changes the partial response transducer 12 into other partial

responses PR (1, 1, -1, -1) which show other predetermined band pass frequency characteristics by the intersymbol interference to odd number sample data among the outputs of A/D converter 116 in ****, as shown in drawing 1 thru/or drawing 15 .

[0029] The magnetic-reproducing decode equipment of this invention is set to ****, as shown in drawing 1 thru/or drawing 15 . Moreover, the phase error detector 1 The inverter circuit 6 which reverses even number sample data from the output of A/D converter 116 to even number sample data only when the polarity of the odd number sample data in front of 1 sample is plus, D/A converter 7 which changes into an analog signal the even number sample data reversed in the inverter circuit 6, It has the gate circuit 8 which outputs the analog signal from D/A converter 7 only when the polarity of the odd number sample data before and behind an even number sample is reversed. A phase error is detected and the sequence of an inverter circuit 6, D/A converter 7, and a gate circuit 8 is changed into arbitration.

[0030] Moreover, the magnetic-reproducing decode equipment of this invention forms the quantization feedback circuit 20 which carries out low-pass amendment of a regenerative signal from the output of the integral equalizer 115 in ****, as shown in drawing 1 thru/or drawing 15 .

[0031] Moreover, as shown in drawing 1 thru/or drawing 15 , the magnetic-reproducing decode equipment of this invention changes to the integral equalizer 115 in ****, and forms the digital equalizer 21 which carries out equivalence of the output of A/D converter 116 to the 1st criteria of nyquist.

[0032]

[Function] Only when the polarity of the odd number sample data of order is reversed from the output of A/D converter 116 to even number sample data according to this invention, it multiplies with the polarity of front odd number sample data. Since the phase error detector 1 which calculates a phase error is formed and the sampling clock of A/D converter 116 was controlled by this phase error output A phase error signal is detectable from the signal of after [A/D conversion] 116. By this Effect is not received in the stability or the error of a time delay of A/D converter 116 and voltage-controlled oscillator 9 grade. It is not necessary to prepare the delay circuit for delay time compensation,

and an exact and stable clock can be obtained. Since it quantizes with the clock which synchronized completely to the signal after integral identification and partial response conversion and Viterbi decoding are performed, it can follow completely to change of a data rate.

[0033] Moreover, according to this invention, in ****, A/D converter 116 and 2nd A/D converter 11 which operates with the sampling clock of opposition are formed. Since it quantizes to odd number sample data with A/D converter 116 and was made to quantize with 2nd A/D converter 11 to even number sample data A/D converter 116 of a main track system, and 2nd A/D converter 11 of a clock extraction system If even strobe delay is equal, you may make it each other quantifying bit numbers differ, and a main track system quantizes with the comparatively fine number of bits, and a clock extraction system can be quantized with the comparatively coarse number of bits, and it can attain improvement in the speed and optimization of equipment.

[0034] Moreover, according to this invention, in ****, since the partial response transducer 12 was changed into other partial responses PR (1, 1, -1, -1) which show other predetermined band pass frequency characteristics by the intersymbol interference to odd number sample data among the outputs of A/D converter 116, it can respond to other partial responses other than partial response class 4PR (1, 0, -1).

[0035] According to this invention, it sets to ****. Moreover, the phase error detector 1 The inverter circuit 6 which reverses even number sample data from the output of A/D converter 116 to even number sample data only when the polarity of the odd number sample data in front of 1 sample is plus, D/A converter 7 which changes into an analog signal the even number sample data reversed in the inverter circuit 6, It has the gate circuit 8 which outputs the analog signal from D/A converter 7 only when the polarity of the odd number sample data before and behind an even number sample is reversed. Since a phase error is detected and the sequence of an inverter circuit 6, D/A converter 7, and a gate circuit 8 was changed into arbitration from the output of a gate circuit 8 In the phase error detector 1, the sequence of an inverter circuit 6, D/A converter 7, and a gate circuit 8 can be constituted in arbitration, and applicability can be extended.

[0036] Moreover, since the quantization feedback circuit 20 which carries out low-pass amendment of a regenerative signal from the output of the integral equalizer 115 was formed in **** according to this invention, effect of cutoff of the low-pass frequency of the regenerative signal by the reproducing head 108 or rotary transformer 114 grade can be lessened, and low-pass amendment of a regenerative signal can be carried out.

[0037] Moreover, since the digital equalizer 21 which changes to the integral equalizer 115 and carries out equivalence of the output of A/D converter 116 to the 1st criteria of nyquist in **** was formed according to this invention, equivalence of the regenerative signal can be carried out to the 1st criteria of nyquist, and that zero cross can detect a clock phase error signal.

[0038]

[Example] Drawing 1 is the block diagram showing the configuration of one example of the magnetic-reproducing decode equipment by this invention. The magnetic-reproducing decode equipment of this invention is characterized by the point which generates the sampling clock of an A/D converter as acquires a phase error signal from the output signal of an A/D converter especially in this example. The applicant of this invention who showed drawing 16 of a Prior art uses in the digital video signal processor for which it applied previously. Since it is the same as usual about the configuration of the digital video signal processor shown in this drawing 16 , that explanation is omitted.

[0039] As shown in drawing 1 , the magnetic-reproducing decode equipment by the example of this invention is constituted as follows. The RF signal reproduced by the reproducing head 108 is supplied and amplified by amplifier 113. The reproducing head 108 and amplifier 113 are formed on the rotating drum which is not illustrated. The regenerative signal amplified with amplifier 113 is supplied to the rotary transformer 114, and is taken out besides a rotating drum. The regenerative signal taken out besides the rotating drum through the rotary transformer 114 is supplied to the integral equalizer 115, and performs data processing of integral identification, i.e., (1+D). Thereby, identification of the regenerative signal is carried out to the 1st criteria of nyquist. The regenerative signal by which integral identification

was carried out is supplied to A/D converter 116, on the basis of a twice as many synchronous clock as a data rate, changes the signal level of a regenerative signal into digital value, and quantizes.

[0040] One side of the digital data quantized with A/D converter 116 is supplied to a computing element (1-D2) 117, and identification is carried out to the partial response class 4 (PR4). Viterbi decoding of the data by which identification was carried out to the partial response class 4 (PR4) is supplied and carried out to the Viterbi decoder 118. Viterbi decoding is a decode method which obtains playback data from the pattern of all state transitions in search of the pattern of a state transition with the highest possibility to a regenerative signal. In VTR using Viterbi decoding, a bit error rate can be improved by decoding a regenerative signal, using the intersymbol interference of input data effectively in the Viterbi decoder.

[0041] (1-D2) One half of 1 / 2 dividing clocks of the synchronous clock supplied to A/D converter 116 are supplied to a computing element 117 and the Viterbi decoder 118 through 1/2 counting-down circuit 10. Thereby, identification of the odd number sample data of the quantized regenerative signal is carried out to the partial response class 4 (PR4) from the 1st criteria of nyquist with a computing element (1-D2) 117, and it is supplied and decoded by the Viterbi decoder 118.

[0042] Here, another side of the digital data quantized with A/D converter 116 is supplied to the phase error detector 1. Within the phase error detector 1, the digital data quantized with A/D converter 116 is supplied to two D flip-flops 2 and 3 which function as a data latch. The most significant bit (MSB) of the input of D flip-flop 2 and the most significant bit (MSB) of the output of D flip-flop 3 are supplied to the IKUSUKURUSHIBUOA circuit 4. The output of the IKUSUKURUSHIBUOA circuit 4, and 1 / 2 dividing clock of 1/2 counting-down circuit 10 are supplied to AND circuit 5. The output of this AND circuit 5 is used as a gate pulse. And the output of D flip-flop 2 is supplied to an inverter circuit 6, and it is reversed by the most significant bit (MSB) of the output of D flip-flop 3. The reversed data are supplied to D/A converter 7, and are changed into an analog value. A phase error output is obtained by supplying the changed analog value to a gate circuit 8, and carrying out the gate by the

gate pulse from AND circuit 5.

[0043] Thus, it restricts, when the polarity of the odd number sample data of order is reverse among the even number sample data of the digital data quantized with A/D converter 116, and D/A conversion of the signal reversed with the polarity of front odd number sample data is carried out, and it is made to take out as a phase error output. That is, when the polarity of the odd number sample data of order is equal, it is made not to output a phase error output, applying the gate.

[0044] This phase error output is supplied to a voltage controlled oscillator 9, and a PLL circuit consists of a phase error detector 1 and a voltage controlled oscillator 9. Thereby, a highly precise synchronous clock is obtained. The synchronous clock generated with the voltage controlled oscillator 9 is supplied to A/D converter 116 and 1/2 counting-down circuit 10. Moreover, a synchronous clock is Clock DFF to the clock input terminal which two D flip-flops 2 and 3 do not illustrate. It is supplied as CK.

[0045] Thus, the synchronous clock which synchronized with A/D-converter 116 output is generated. The data in A/D converter 116 are sampled with this synchronous clock, applying phase simulation, and it is made to perform the operation and decode in a computing element (1-D2) 117 and the Viterbi decoder 118. This becomes possible also to fluctuation of not only the jitter of VTR but the data rate at the time of a search to obtain an exact and stable clock.

[0046] Drawing 2 is drawing showing the eye pattern of one example of the magnetic-reproducing decode equipment of this invention. This eye pattern is the same as that of the eye pattern of PR playback decoder circuit for which the applicant of this invention who showed drawing 19 applied previously. An eye pattern says drawing which wrote the regenerative-signal wave after identification in piles the detecting point period (data rate), and the situation of the intersymbol interference of an identification signal is investigated. The eye pattern which the eye pattern shown in drawing 2 A shows the eye pattern after the integral identification by the integral equalizer 115 shown in drawing 1 , and is shown in drawing 2 B shows the eye pattern after the identification by the computing element 117 shown in drawing 2 (1-D2) (1-D2). The phase

error detector 1 shown in drawing 1 supplies a phase error output to a voltage controlled oscillator 9, and he is trying to generate a synchronous clock with a voltage controlled oscillator 9 by detecting this zero cross.

[0047] Drawing 3 is drawing showing the signal wave form at the time of the clock phase lock of one example of the magnetic-reproducing decode equipment of this invention. Drawing 3 A shows a synchronous clock, drawing 3 B shows 1 / 2 dividing clock, drawing 3 C shows an integral equalizer output, drawing 3 D shows an A/D-converter output, drawing 3 E shows D-flip-flop 2 output, drawing 3 F shows D-flip-flop 3 output, drawing 3 G shows an AND circuit output, and drawing 3 H shows a phase error detector output (gate circuit output).

[0048] Drawing 4 is drawing showing the signal wave form at the time of the clock phase lead lag network of one example of the magnetic-reproducing decode equipment of this invention. Drawing 4 A shows a synchronous clock, drawing 4 B shows 1 / 2 dividing clock, drawing 4 C shows an integral equalizer output, drawing 4 D shows an A/D-converter output, drawing 4 E shows D-flip-flop 2 output, drawing 4 F shows D-flip-flop 3 output, drawing 4 G shows an AND circuit output, and drawing 4 H shows a phase error detector output.

[0049] To a phase error detector output being zero as shown in drawing 3 H at the time of a clock phase lock, at the time of a clock phase lead lag network, as shown in drawing 4 H, the pulse of minus of a phase error detector output (gate circuit output) to the timing of a gate circuit was outputted, and the clock phase lead lag network is detected.

[0050] Drawing 11 is drawing showing the phase drawing-in property over the M sequence signal which carried out integral equalization in the roll-off 0.5 of one example of the magnetic-reproducing decode equipment of this invention. An axis of abscissa shows time amount to the sample number of bits of an A/D converter, i.e., an indirect target. An axis of ordinate shows the phase error over clock period T of a synchronous clock. - 0.5T mean that only the half period was overdue to clock period T of a synchronous clock, and show the worst phase lag condition. Phase **** after drawing, being stabilized and drawing further with the sample number of bits of about 150 bits only is also a

peak TSUUPIKU value, and is a minute amount very much with 1 or less %.
[0051] Only when the polarity of the odd number sample data of order is reversed from the output of A/D converter 116 to even number sample data according to the upper example, it multiplies with the polarity of front odd number sample data. Since the phase error detector 1 which calculates a phase error is formed and the sampling clock of A/D converter 116 was controlled by this phase error output A phase error signal is detectable from the signal of after [A/D conversion] 116. By this Effect is not received in the stability or the error of a time delay of A/D converter 116 and voltage-controlled oscillator 9 grade. It is not necessary to prepare the delay circuit for delay time compensation, and an exact and stable clock can be obtained. Since it quantizes with the clock which synchronized completely to the signal after integral identification and partial response conversion and Viterbi decoding are performed, it can follow completely to change of a data rate.
[0052] Drawing 5 is the block diagram showing the configuration of other examples of the magnetic-reproducing decode equipment by this invention. In this example, it is characterized by the point of operating an A/D converter with the clock of the non-inverter of a data rate, and opposition especially by dividing into two. As shown in drawing 5 , the magnetic-reproducing decode equipment by other examples of this invention is constituted as follows. The RF signal reproduced by the reproducing head 108 is supplied and amplified by amplifier 113. The reproducing head 108 and amplifier 113 are formed on the rotating drum which is not illustrated. The regenerative signal amplified with amplifier 113 is supplied to the rotary transformer 114, and is taken out besides a rotating drum. The regenerative signal taken out besides the rotating drum through the rotary transformer 114 is supplied to the integral equalizer 115, and performs data processing of integral identification, i.e., (1+D). Thereby, identification of the regenerative signal is carried out to the 1st criteria of nyquist. The regenerative signal by which integral identification was carried out is supplied to A/D converter 116, on the basis of the synchronous clock of the non-inverter of a data rate, changes the signal level of a regenerative signal into digital value, and quantizes.
[0053] One side of the digital data quantized with A/D converter 116 is

supplied to a computing element (1-D2) 117, and identification is carried out to the partial response class 4 (PR4). Viterbi decoding of the data by which identification was carried out to the partial response class 4 (PR4) is supplied and carried out to the Viterbi decoder 118. Viterbi decoding is a decode method which obtains playback data from the pattern of all state transitions in search of the pattern of a state transition with the highest possibility to a regenerative signal. In VTR using Viterbi decoding, a bit error rate can be improved by decoding a regenerative signal, using the intersymbol interference of input data effectively in the Viterbi decoder.

[0054] (1-D2) The synchronous clock of the non-inverter supplied to A/D converter 116 is supplied also to a computing element 117 and the Viterbi decoder 118. Thereby, identification of the odd number sample data of the quantized regenerative signal is carried out to the partial response class 4 (PR4) from the 1st criteria of nyquist with a computing element (1-D2) 117, and it is supplied and decoded by the Viterbi decoder 118.

[0055] Here, another side of the digital data quantized with A/D converter 116 is supplied to the phase error detector 1. Within the phase error detector 1, the digital data quantized with A/D converter 116 is supplied to D flip-flop 2 which functions as a data latch. The most significant bit of digital data and the most significant bit (MSB) of the output of D flip-flop 2 which were supplied from A/D converter 116 are supplied to the IKUSUKURUSHIBUOA circuit 4. The output and non-inverter clock of the IKUSUKURUSHIBUOA circuit 4 are supplied to AND circuit 5. The output of this AND circuit 5 is used as a gate pulse.

[0056] And another side of the regenerative signal supplied from the integral equalizer 115 is supplied to A/D converter 11. A/D converter 11 changes the signal level of a regenerative signal into digital value for a regenerative signal on the basis of the synchronous clock of the opposition of a data rate. The changed digital data is supplied to an inverter circuit 6, and is reversed by the most significant bit (MSB) of the output of D flip-flop 2. The reversed data are supplied to D/A converter 7, and are changed into an analog value. A phase error output is obtained by supplying the changed analog value to a gate circuit 8, and carrying out the gate by the gate pulse from AND circuit 5.

[0057] Thus, an integral identification output is supplied to A/D converter 116 and A/D converter 11. It quantizes with the non-inverter clock of a data rate, and A/D converter 116 passes along a computing element (1-D2) 117 and the Viterbi decoder 118, and serves as playback data. Moreover, IKUSUKURUSHIBUOA of the most significant bit (MSB) of A/D converter 116 and the data of 1 clock delay of this most significant bit (MSB) is taken, ANDO with a non-inverter clock is taken further, and a gate pulse is made.

[0058] On the other hand, after quantizing A/D converter 11 with the clock of the opposition of a data rate and being reversed by the most significant bit (MSB) which carried out 1 clock delay, D/A conversion was carried out and the phase error output has been obtained by applying the gate by the gate pulse.

[0059] Thus, the clock phase error output used as the same effectiveness as the example shown in drawing 1 is detectable by operating an A/D converter with the clock of the non-inverter of a data rate, and opposition by dividing into two. Drawing 6 is drawing showing the signal wave form of other examples of the magnetic-reproducing decode equipment of this invention. Drawing 6 A shows a non-inverter clock, drawing 6 B shows an opposition clock, drawing 6 C shows an integral equalizer output, drawing 6 D shows A/D-converter 116 output, drawing 6 E shows D-flip-flop 2 output, drawing 6 F shows A/D-converter 117 output, drawing 6 G shows an AND circuit output, and drawing 6 H shows a phase error detector output (gate circuit output).

[0060] In drawing 6 , to a phase error detector output being zero as shown in drawing 3 H at the time of a clock phase lock, as shown in drawing 6 H, the pulse of minus of a phase error detector output (gate circuit output) to the timing of a gate circuit was outputted, and the clock phase lead lag network is detected at the time of a clock phase lead lag network. Moreover, it returns to drawing 5 and a non-inverter clock is supplied to the clock input terminal which D flip-flop 2 does not illustrate.

[0061] Thus, the non-inverter clock which synchronized with A/D-converter 116 output is generated. The data in A/D converter 116 are sampled with this non-inverter clock, applying phase simulation, and it is made to perform the operation and decode in a computing element (1-D2) 117 and the Viterbi

decoder 118. This becomes possible also to fluctuation of not only the jitter of VTR but the data rate at the time of a search to obtain an exact and stable clock.

[0062] Furthermore, as long as even the strobe delay of A/D converter 116 and A/D converter 11 is equal, the numbers of bits may differ. Drawing 12 is drawing showing the phase drawing-in property over the M sequence signal which carried out integral equalization in the roll-off 0.5 of other examples of the magnetic-reproducing decode equipment of this invention. The axis of abscissa and the axis of ordinate are the same as what was shown in drawing 11 . In drawing 12 , when quantifying bit numbers are 1 thru/or 2, much phase ****** are accepted, but when quantifying bit numbers are 3 thru/or 4, it turns out that there is very little phase ******.

[0063] Therefore, in drawing 5 , when a quantifying bit number attains improvement in the speed of equipment using the thing of 6, a quantifying bit number attains optimization to A/D converter 11 of a phase detection system using the thing of 3 thru/or 4 and it operates with a 200MHz thump RINNGU clock to A/D converter 116 of a main track system, respectively, it will be equivalent to 400MHz by two. Generally, as for A/D converter 11 of a phase detection system, A/D converter 116 of a main track system is known by that at least 4 bits are 1 or less %, and the peak two peak value of phase ****** is held down for them by the sufficiently small jitter although about 6 bits of quantifying bit numbers are called need.

[0064] According to the upper example, in ****, A/D converter 116 and 2nd A/D converter 11 which operates with the sampling clock of opposition are formed. Since it quantizes to odd number sample data with A/D converter 116 and was made to quantize with 2nd A/D converter 11 to even number sample data A/D converter 116 of a main track system, and 2nd A/D converter 11 of a clock extraction system If even strobe delay is equal, you may make it each other quantifying bit numbers differ, and a main track system quantizes with the comparatively fine number of bits, and a clock extraction system can be quantized with the comparatively coarse number of bits, and it can attain improvement in the speed and optimization of equipment.

[0065] Drawing 7 is the block diagram showing the configuration of other

examples of the magnetic-reproducing decode equipment by this invention. As shown in drawing 7 , the magnetic-reproducing decode equipment by other examples of this invention is constituted as follows. Especially in this example, it is characterized by the point of equalizing playback data in PR (1, 1, -1, -1), as partial responses other than partial response class 4 (PR4).

[0066] As shown in drawing 7 , the magnetic-reproducing decode equipment by the example of this invention is constituted as follows. The RF signal reproduced by the reproducing head 108 is supplied and amplified by amplifier 113. The reproducing head 108 and amplifier 113 are formed on the rotating drum which is not illustrated. The regenerative signal amplified with amplifier 113 is supplied to the rotary transformer 114, and is taken out besides a rotating drum. The regenerative signal taken out besides the rotating drum through the rotary transformer 114 is supplied to the integral equalizer 115, and identification of the regenerative signal is carried out to the 1st criteria of nyquist by this which performs data processing of integral identification, i.e., (1+D). The regenerative signal by which integral identification was carried out is supplied to A/D converter 116, on the basis of a twice as many synchronous clock as a data rate, changes the signal level of a regenerative signal into digital value, and quantizes.

[0067] One side of the digital data quantized with A/D converter 116 is supplied to a computing element (1+D-D2-D3) 12, and identification is carried out to a partial response PR (1, 1, -1, -1). Viterbi decoding of the data by which identification was carried out to the partial response PR (1, 1, -1, -1) is supplied and carried out to the Viterbi decoder 118. Viterbi decoding is a decode method which obtains playback data from the pattern of all state transitions in search of the pattern of a state transition with the highest possibility to a regenerative signal. In VTR using Viterbi decoding, a bit error rate can be improved by decoding a regenerative signal, using the intersymbol interference of input data effectively in the Viterbi decoder.

[0068] (1+D-D2-D3) One half of 1 / 2 dividing clocks of the synchronous clock supplied to A/D converter 116 are supplied to a computing element 12 and the Viterbi decoder 118 through 1/2 counting-down circuit 10. Thereby, identification of the odd number sample data of the quantized regenerative

signal is carried out to a partial response PR (1, 1, -1, -1) from the 1st criteria of nyquist with a computing element (1+D-D2-D3) 12, and it is supplied and decoded by the Viterbi decoder 118.

[0069] Here, another side of the digital data quantized with A/D converter 116 is supplied to the phase error detector 1. Within the phase error detector 1, the digital data quantized with A/D converter 116 is supplied to two D flip-flops 2 and 3 which function as a data latch. The most significant bit (MSB) of the input of D flip-flop 2 and the most significant bit (MSB) of the output of D flip-flop 3 are supplied to the IKUSUKURUSHIBUOA circuit 4. The output of the IKUSUKURUSHIBUOA circuit 4, and 1 / 2 dividing clock of 1/2 counting-down circuit 10 are supplied to AND circuit 5. The output of this AND circuit 5 is used as a gate pulse. And the output of D flip-flop 2 is supplied to an inverter circuit 6, and it is reversed by the most significant bit (MSB) of the output of D flip-flop 3. The reversed data are supplied to D/A converter 7, and are changed into an analog value. A phase error output is obtained by supplying the changed analog value to a gate circuit 8, and carrying out the gate by the gate pulse from AND circuit 5.

[0070] Thus, it restricts, when the polarity of the odd number sample data of order is reverse among the even number sample data of the digital data quantized with A/D converter 116, and D/A conversion of the signal reversed with the polarity of front odd number sample data is carried out, and it is made to take out as a phase error output. That is, when the polarity of the odd number sample data of order is equal, it is made not to output a phase error output, applying the gate.

[0071] This phase error output is supplied to a voltage controlled oscillator 9, and a PLL circuit consists of a phase error detector 1 and a voltage controlled oscillator 9. Thereby, a highly precise synchronous clock is obtained. The synchronous clock generated with the voltage controlled oscillator 9 is supplied to A/D converter 116 and 1/2 counting-down circuit 10. Moreover, a synchronous clock is Clock DFF to the clock input terminal which two D flip-flops 2 and 3 do not illustrate. It is supplied as CK.

[0072] Thus, the synchronous clock which synchronized with A/D-converter 116 output is generated. The data in A/D converter 116 are sampled with this

synchronous clock, applying phase simulation, and it is made to perform the operation and decode in a computing element (1+D-D2-D3) 12 and the Viterbi decoder 118. This becomes possible also to fluctuation of not only the jitter of VTR but the data rate at the time of a search to obtain an exact and stable clock.

[0073] Drawing 8 is the block diagram showing the configuration of the computing element (1+D-D2-D3) of other examples of the magnetic-reproducing decode equipment by this invention. As shown in drawing 8 , a computing element (1+D-D2-D3) consists of a converter (1-D2) 13 and a converter (1+D) 17. In drawing 8 , one side of an input signal is supplied to one input terminal of a subtractor 16 through D flip-flop 14 and D flip-flop 15 in a converter (1-D2) 13, and another side of an input signal is supplied to the input terminal of another side of a subtractor 16, and subtracts the input signal in front of 2 clocks, and the present input signal.

[0074] One side of the signal of the subtracted result is supplied to one input terminal of an adder 19 through D flip-flop 18 in a converter (1+D) 17, and another side of a signal is supplied to the input terminal of another side of an adder 19, adds the signal in front of 1 clock, and a current signal, and considers them as a conversion output.

[0075] Thus, it is (1-D2) *(1+D) =1+D-D2-D3 by the converter (1-D2) 13 and the converter (1+D) 17. It is made to calculate. In addition, other configurations may be used as long as not the thing to restrict to this configuration but the same result is obtained.

[0076] According to the upper example, it sets to ****, and is 1+D-D2-D3 as a partial response converter. A computing element 12 Since it was made to change into other partial responses PR (1, 1, -1, -1) which show other predetermined band pass frequency characteristics by the intersymbol interference to odd number sample data among the outputs of A/D converter 116 It can respond to other partial responses other than partial response class 4PR (1, 0, -1).

[0077] Drawing 9 is the block diagram showing the configuration of other examples of the magnetic-reproducing decode equipment by this invention. As shown in drawing 9 , the magnetic-reproducing decode equipment by other

examples of this invention is constituted as follows. Especially in this example, it is characterized by the point of having replaced the sequence of D/A converter 7 in the phase error detector 1 in a phase detection system, an inverter circuit 6, and a gate circuit 8. This sequence may be changed not only to what was shown in drawing 9 but to arbitration. Since other configurations in a main track system are the same as that of what was shown in drawing 1 , the detailed explanation is omitted.

[0078] In drawing 9 , another side of the digital data quantized with A/D converter 116 is supplied to the phase error detector 1. Within the phase error detector 1, the digital data quantized with A/D converter 116 is supplied to two D flip-flops 2 and 3 which function as a data latch. The most significant bit (MSB) of the input of D flip-flop 2 and the most significant bit (MSB) of the output of D flip-flop 3 are supplied to the IKUSUKURUSHIBUOA circuit 4. The output of the IKUSUKURUSHIBUOA circuit 4, and 1 / 2 dividing clock of 1/2 counting-down circuit 10 are supplied to AND circuit 5. The output of this AND circuit 5 is used as a gate pulse. And the output of D flip-flop 2 is supplied to D/A converter 7, and it changes into an analog value. The changed analog value is supplied to an inverter circuit 6, and it is reversed by the most significant bit (MSB) of the output of D flip-flop 3. A phase error output is obtained by supplying the reversed analog value to a gate circuit 8, and carrying out the gate by the gate pulse from AND circuit 5.

[0079] According to the upper example, it sets to ****. The phase error detector 1 D/A converter 7 which changes even number sample data into an analog signal from the output of A/D converter 116, The inverter circuit 6 which makes the output of D/A converter 7 the polarity of the odd number sample data in front of 1 sample, Since it has the gate circuit 8 which carries out the gate of the output signal of an inverter circuit 6, a phase error is detected from a gate circuit 8 and the sequence of an inverter circuit 6, D/A converter 7, and a gate circuit 8 was changed into arbitration In the phase error detector 1, the sequence of an inverter circuit 6, D/A converter 7, and a gate circuit 8 can be constituted in arbitration, and applicability can be extended.

[0080] Drawing 10 is the block diagram showing the configuration of other

examples of the magnetic-reproducing decode equipment by this invention. As shown in drawing 10 , the magnetic-reproducing decode equipment by other examples of this invention is constituted as follows. Especially in this example, in order to mitigate low-pass cutoff of the regenerative signal by rotary transformer 114 grade, it is characterized by the point of having established the quantization feedback circuit 20 in the preceding paragraph of A/D converter 116 of a main track system. As long as this quantization feedback circuit 20 has the function which amends the low-pass component of not only a thing but the regenerative signal shown in drawing 10 , other things are sufficient as it. Since other configurations in a phase detection system are the same as that of what was shown in drawing 1 , the detailed explanation is omitted.

[0081] With VTR, low-pass cutoff of the frequency of the regenerative signal by the reproducing head 108 and rotary transformer 114 grade exists. The regenerative signal by which identification was carried out to the 1st criteria of nyquist with the integral equalizer 115 is supplied to the quantization feedback circuit 20 so that the effect of this low-pass cutoff may be mitigated. The quantization feedback circuit 20 serves to reproduce the low-pass component of a regenerative signal. Thereby, the effect of low-pass cutoff is mitigable.

[0082] Drawing 13 is drawing showing the phase drawing-in property over the M sequence signal which carried out integral equalization in the roll-off 0.5 of other examples of the magnetic-reproducing decode equipment of this invention. The axis of abscissa and the axis of ordinate are the same as what was shown in drawing 11 and drawing 12 . It turns out that there is little phase ****** in drawing 13 when there is no low frequency cutoff, but phase ****** increases, so that phase ****** becomes somewhat large when low frequency cutoff is 0.03 times the Nyquist rate, phase ****** becomes larger and low frequency cutoff becomes high, when low frequency cutoff is 0.1 times the Nyquist rate. Here, the convergence value has changed, because the group delay has changed by low-pass cutoff, and there is especially no problem. A group delay is a function showing the amount of delay in a certain frequency.

[0083] Since the quantization feedback circuit 20 which carries out low-pass amendment of a regenerative signal from the output of the integral equalizer

115 was formed in **** according to the upper example, effect of cutoff of the low-pass frequency of the regenerative signal by the reproducing head 108 or rotary transformer 114 grade can be lessened, and low-pass amendment of a regenerative signal can be carried out.

[0084] Drawing 14 is the block diagram showing the configuration of other examples of the magnetic-reproducing decode equipment by this invention. As shown in drawing 14 , the magnetic-reproducing decode equipment by other examples of this invention is constituted as follows. Especially in this example, it is characterized by the point of having changed to the integral equalizer 115 and having formed the digital equalizer 21 in the latter part of A/D converter 116 of a main track system. As long as this digital equalizer 21 suppresses the effect on the playback data based on the temperature characteristic and variation of not only a thing but an analog equalizer which were shown in drawing 14 , other things are sufficient as it. Since other configurations in a phase detection system are the same as that of what was shown in drawing 1 , the detailed explanation is omitted.

[0085] The playback data changed into digital value by A/D converter 116 of a main track system are supplied to the digital equalizer 21. The digital equalizer 21 consists of FIR filters, IIR filters, etc. as a digital filter. The digital equalizer 21 equalizes playback data on the 1st criteria of nyquist. Since identification of the 1st criteria of nyquist is performed in digital one, the effect on the playback data based on the temperature characteristic and variation of an analog equalizer can be suppressed.

[0086] Drawing 15 is drawing showing the signal wave form for explaining radical Motohara ** of the phase error detector of the magnetic-reproducing decode equipment by this invention. As shown in drawing 15 , the odd number sample when sampling with a twice as many clock as a data rate is made into o1, o2, o3, and ... with A/D converter 116, and an even number sample is made into e1, e2, e3, and ... Therefore, from A/D converter 116, the electrical potential difference of a regenerative signal shall be sampled in order of o1, e1, o2, e2, o3, e3, and ... In NRZ, an odd number sample is a detecting point, or the electrical potential difference of this point is higher than zero or low, it is, and 0 and 1 are decoded.

[0087] On the other hand, in drawing 15 , the polarity as a detection value of the sample o2 in front of one considers the case where the sample o3 after one is (+) in (-) like e2. If identification of the electrical potential difference of a regenerative signal is carried out to the 1st criteria of nyquist, as for e2, a clock phase will serve as near zero potential at the time of the right. If the clock phase has shifted, the potential of e2 will fall to clock progress, and the potential of e2 will go up to clock delay.

[0088] Moreover, like e4, when the sample of order is changing from (+) to (-), it is contrary to the case of e2, and to clock progress, the potential of e4 goes up and falls to delay.

[0089] Therefore, the thing by which the polarity of the odd number sample before and behind that is changing from (-) to (+) among even number samples, It is reversing a polarity to what detects what is changing from (+) to (-), outputs as it is to what is changing from (-) to (+), and is changing from (+) to (-). In any case, to negative clock delay, a forward electrical potential difference is detectable to clock progress.

[0090] Since the digital equalizer 21 which changes to the integral equalizer 115 and carries out equivalence of the output of A/D converter 116 to the 1st criteria of nyquist in **** was formed according to the upper example, equivalence of the regenerative signal can be carried out to the 1st criteria of nyquist, and a clock phase error signal can be detected.

[0091]

[Effect of the Invention] Only when the polarity of the odd number sample data of order is reversed from the output of an A/D converter to even number sample data according to this invention, it multiplies with the polarity of front odd number sample data. Since the phase error detector which calculates a phase error is formed and the sampling clock of an A/D converter was controlled by this phase error output A phase error signal is detectable from the signal after A/D conversion. By this Effect is not received in the stability or the error of a time delay of an A/D converter, a voltage-controlled oscillator, etc. It is not necessary to prepare the delay circuit for delay time compensation, and an exact and stable clock can be obtained. Since it quantizes with the clock which synchronized completely to the signal after

integral identification and partial response conversion and Viterbi decoding are performed, it can follow completely to change of a data rate.

[0092] Moreover, according to this invention, in ****, an A/D converter and the 2nd A/D converter which operates with the sampling clock of opposition are formed. Since it quantizes to odd number sample data with an A/D converter and was made to quantize with the 2nd A/D converter to even number sample data The A/D converter of a main track system, and the 2nd A/D converter of a clock extraction system If even strobe delay is equal, you may make it each other quantifying bit numbers differ, and a main track system quantizes with the comparatively fine number of bits, and a clock extraction system can be quantized with the comparatively coarse number of bits, and it can attain improvement in the speed and optimization of equipment.

[0093] Moreover, according to this invention, in ****, since the partial response transducer was changed into other partial responses which show other predetermined band pass frequency characteristics by the intersymbol interference to odd number sample data among the outputs of an A/D converter, it can respond to other partial responses other than a specific partial response.

[0094] According to this invention, it sets to ****. Moreover, a phase error detector The inverter circuit which has even number sample data reversed from the output of an A/D converter to even number sample data only when the polarity of the odd number sample data in front of 1 sample is plus, The D/A converter which changes into an analog signal the even number sample data reversed in the inverter circuit, It has the gate circuit which carries out the gate of the analog signal from a D/A converter only when the polarity of the odd number sample data before and behind an even number sample is reversed. Since a phase error is detected and the sequence of an inverter circuit, a D/A converter, and a gate circuit was changed into arbitration from the gate circuit In a phase error detector, the sequence of an inverter circuit, a D/A converter, and a gate circuit can be constituted in arbitration, and applicability can be extended.

[0095] Moreover, since the quantization feedback circuit which carries out low-pass amendment of a regenerative signal from the output of an integral

equalizer was prepared in **** according to this invention, effect of cutoff of the low-pass frequency of the regenerative signal by the reproducing head, a rotary transformer, etc. can be lessened, and low-pass amendment of a regenerative signal can be carried out.

[0096] Moreover, since the digital equalizer which changes to an integral equalizer and carries out equivalence of the output of an A/D converter to the 1st criteria of nyquist in **** was formed according to this invention, equivalence of the regenerative signal can be carried out to the 1st criteria of nyquist, and a clock phase error signal can be detected.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the configuration of one example of the magnetic-reproducing decode equipment of this invention.

[Drawing 2] It is drawing showing the eye pattern of one example of the magnetic-reproducing decode equipment of this invention, drawing 2 A shows the eye pattern after integral identification, and drawing 2 B is 1-D2. It is drawing showing the eye pattern after identification.

[Drawing 3] It is drawing showing the signal wave form at the time of the clock phase lock of one example of the magnetic-reproducing decode equipment of this invention. Drawing 3 A shows a synchronous clock and drawing 3 B shows 1 / 2 dividing clock. Drawing 3 C shows an integral equalizer output, drawing 3 D shows an A/D-converter output, drawing 3 E shows D-flip-flop 2 output, drawing 3 F shows D-flip-flop 3 output, drawing 3 G shows an AND circuit output, and drawing 3 H is drawing showing a phase error detector output (gate circuit output).

[Drawing 4] It is drawing showing the signal wave form at the time of the clock phase lead lag network of one example of the magnetic-reproducing decode equipment of this invention. Drawing 4 A shows a synchronous clock and

drawing 4 B shows 1 / 2 dividing clock. Drawing 4 C shows an integral equalizer output, drawing 4 D shows an A/D-converter output, drawing 4 E shows D-flip-flop 2 output, drawing 4 F shows D-flip-flop 3 output, drawing 4 G shows an AND circuit output, and drawing 4 H is drawing showing a phase error detector output (gate circuit output).

[Drawing 5] It is the block diagram showing the configuration of other examples of the magnetic-reproducing decode equipment of this invention.

[Drawing 6] It is drawing showing the signal wave form of other examples of the magnetic-reproducing decode equipment of this invention, drawing 6 A shows a non-inverter clock, drawing 6 B shows an opposition clock, drawing 6 C shows an integral equalizer output, drawing 6 D shows A/D-converter 116 output, drawing 6 E shows a D-flip-flop output, drawing 6 F shows A/D-converter 117 output, drawing 6 G shows an AND circuit output, and drawing 6 H is drawing shown in a phase error detector output (gate circuit output).

[Drawing 7] It is the block diagram showing the configuration of other examples of the magnetic-reproducing decode equipment of this invention.

[Drawing 8] It is the block diagram showing the configuration of the computing element (1+D-D2-D3) of other examples of the magnetic-reproducing decode equipment of this invention.

[Drawing 9] It is the block diagram showing the configuration of other examples of the magnetic-reproducing decode equipment of this invention.

[Drawing 10] It is the block diagram showing the configuration of other examples of the magnetic-reproducing decode equipment of this invention.

[Drawing 11] It is drawing showing the phase drawing-in property over the M sequence signal which carried out integral equalization in the roll-off 0.5 of one example of the magnetic-reproducing decode equipment of this invention.

[Drawing 12] It is drawing showing the phase drawing-in property over the M sequence signal which carried out integral equalization in the roll-off 0.5 of other examples of the magnetic-reproducing decode equipment of this invention.

[Drawing 13] It is drawing showing the phase drawing-in property over the M sequence signal which carried out integral equalization in the roll-off 0.5 of other examples of the magnetic-reproducing decode equipment of this

invention.

[Drawing 14] It is the block diagram showing the configuration of other examples of the magnetic-reproducing decode equipment of this invention.

[Drawing 15] It is drawing showing the signal wave form for explaining radical Motohara ** of the phase error detector of the magnetic-reproducing decode equipment of this invention.

[Drawing 16] It is the block diagram of the digital video signal processor for which the applicant of this invention applied previously.

[Drawing 17] It is drawing showing PR4 playback decoder circuit for which the applicant of this invention applied previously.

[Drawing 18] It is drawing showing the signal wave form of PR4 playback decoder circuit for which the applicant of this invention applied previously. Drawing 18 A shows record data, drawing 18 B shows a PURIKODO output, and drawing 18 C shows 2-bit delay of a PURIKODO output. Drawing 18 D shows a reproducing-head output, drawing 18 E shows an integral equalizer output, drawing 18 F shows a playback clock, drawing 18 G shows 2-bit delay of an integral equalizer output, and drawing 18 H is 1-D2. It is drawing showing a computing-element output.

[Drawing 19] It is drawing showing the eye pattern of PR4 playback decoder circuit for which the applicant of this invention applied previously, drawing 19 A shows the eye pattern after integral identification, and drawing 19 B is 1-D2. It is drawing showing the eye pattern after identification.

[Drawing 20] It is drawing showing the actual configuration of PR4 playback decoder circuit for which the applicant of this invention applied previously.

[Drawing 21] It is drawing showing the amount of delay in the actual configuration of PR4 playback decoder circuit for which the applicant of this invention applied previously, and drawing 21 A shows an integral equalizer output, drawing 21 B shows a limiter output, drawing 21 C shows a PLL circuit output, and drawing 21 D is drawing showing an A/D-converter output.

[Description of Notations]

1 Phase Error Detector

2 D Flip-flop

3 D Flip-flop

4 IKUSUKURUSHIBUOA Circuit

5 AND Circuit

6 Inverter Circuit

7 D/A Converter

8 Gate Circuit

9 VCO

10 1/2 Counting-down Circuit

11 A/D Converter

12 1+D-D2-D3 Computing Element

13 1-D2 Converter

14 D Flip-flop

15 D Flip-flop

16 Subtractor

17 1+D Converter

18 D Flip-flop

19 Adder

20 Quantization Feedback Circuit

21 Digital Equalizer